FIG.1

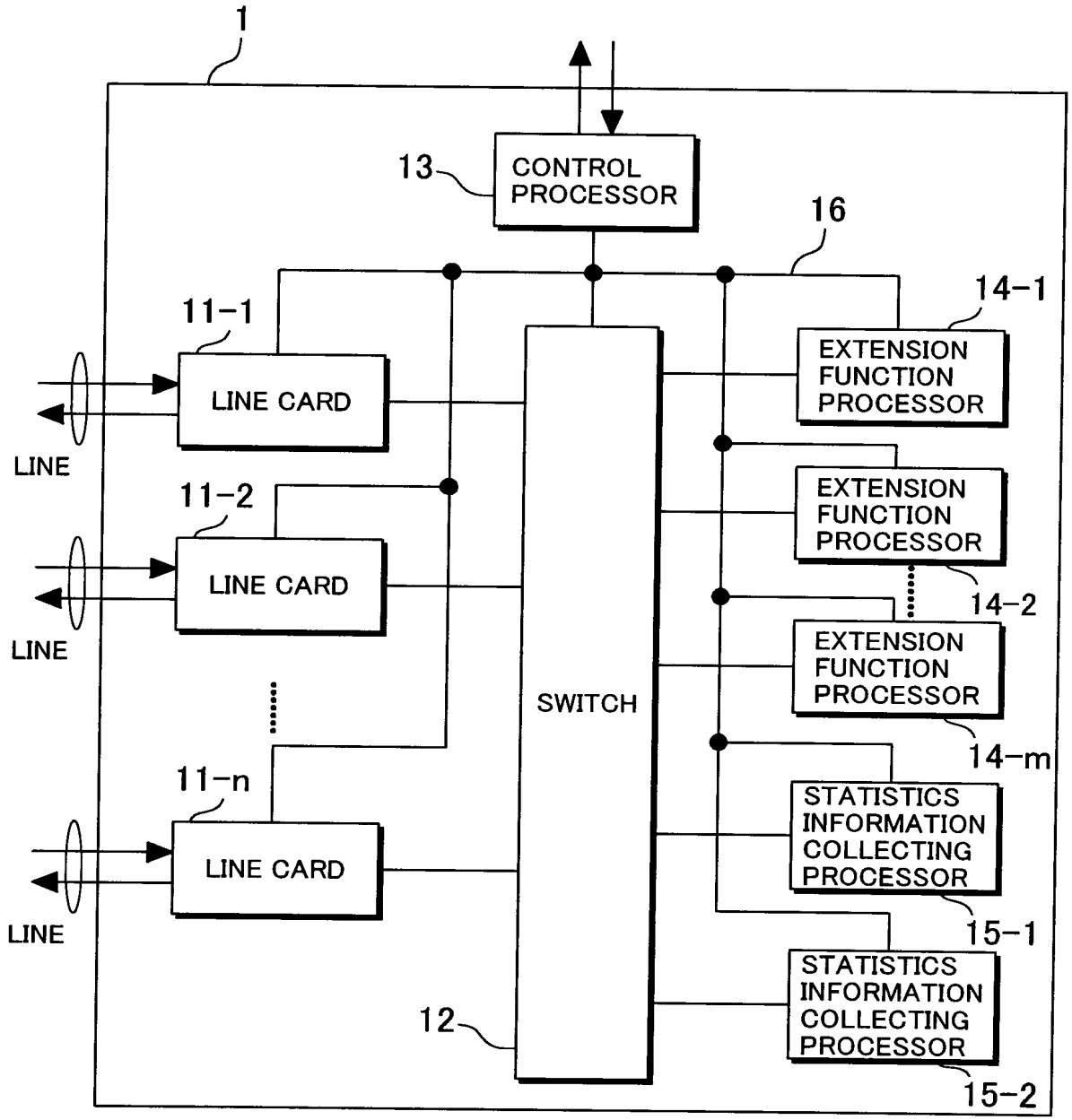

1
13
CONTROL PROCESSOR
16
11-1
LINE CARD
LINE
11-2
LINE CARD
LINE
11-n
LINE CARD
LINE
SWITCH
12
14-1
EXTENSION FUNCTION PROCESSOR
EXTENSION FUNCTION PROCESSOR
14-2
EXTENSION FUNCTION PROCESSOR
14-m
STATISTICS INFORMATION COLLECTING PROCESSOR
15-1
STATISTICS INFORMATION COLLECTING PROCESSOR
15-2

FIG.2

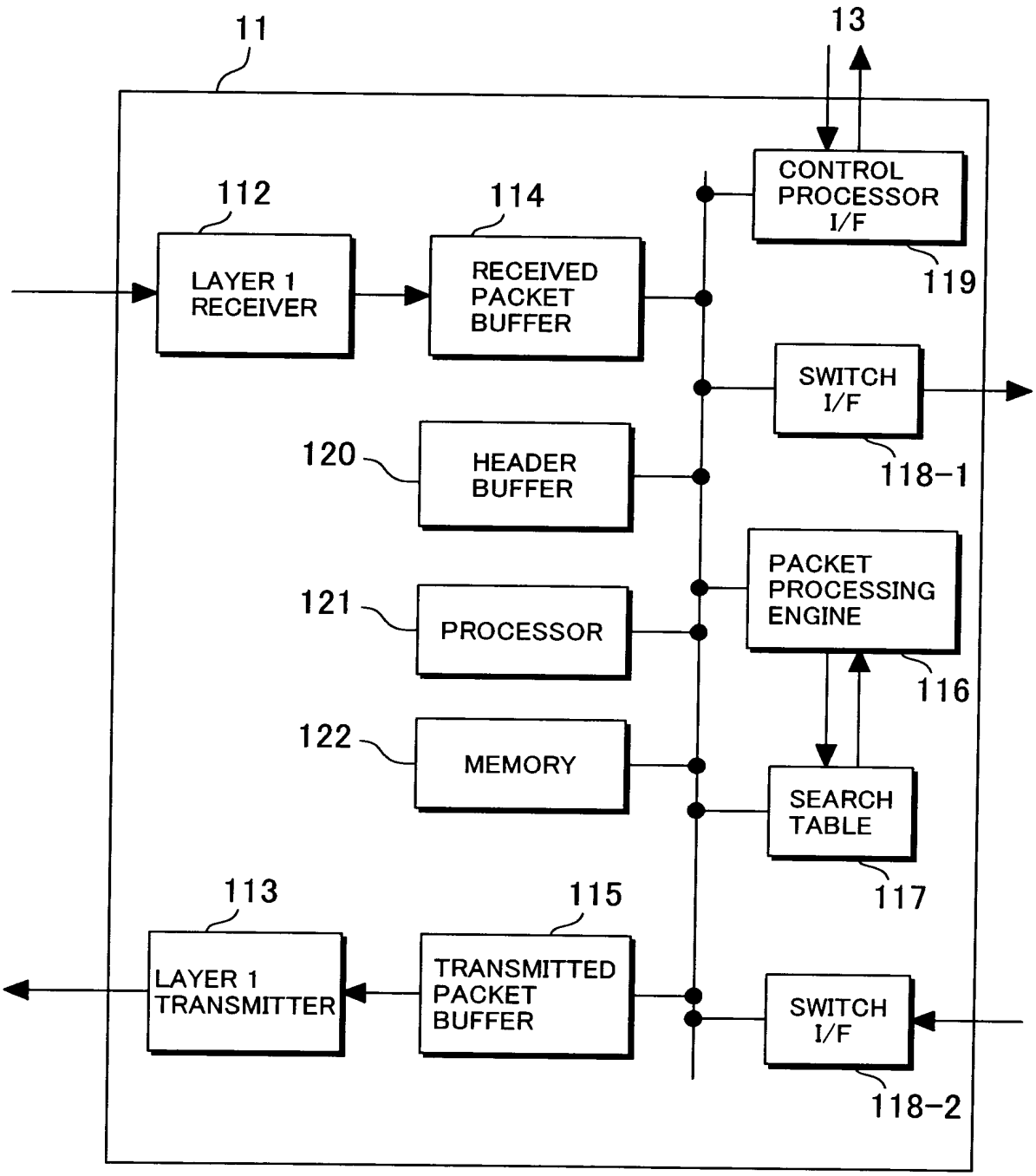

11
13
CONTROL PROCESSOR I/F
119
112
LAYER 1 RECEIVER
114
RECEIVED PACKET BUFFER
SWITCH I/F
118-1
120
HEADER BUFFER
PACKET PROCESSING ENGINE
116
121
PROCESSOR
122
MEMORY
SEARCH TABLE
117
113
LAYER 1 TRANSMITTER
115
TRANSMITTED PACKET BUFFER
SWITCH I/F
118-2

FIG.3

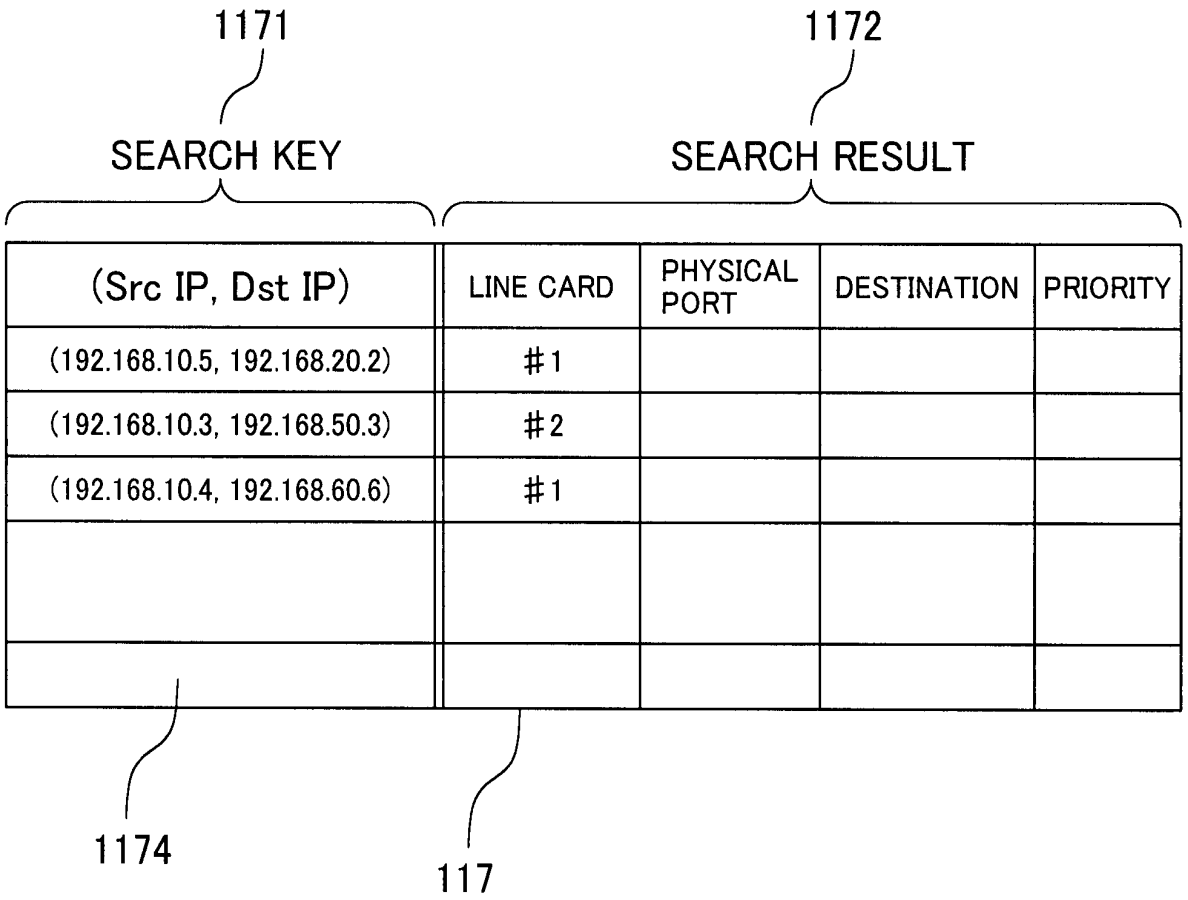

1171
1172
SEARCH KEY
SEARCH RESULT
(Src IP, Dst IP)
LINE CARD
PHYSICAL PORT
DESTINATION
PRIORITY
(192.168.10.5, 192.168.20.2)
#1
(192.168.10.3, 192.168.50.3)
#2
(192.168.10.4, 192.168.60.6)
#1
1174
117

FIG.4

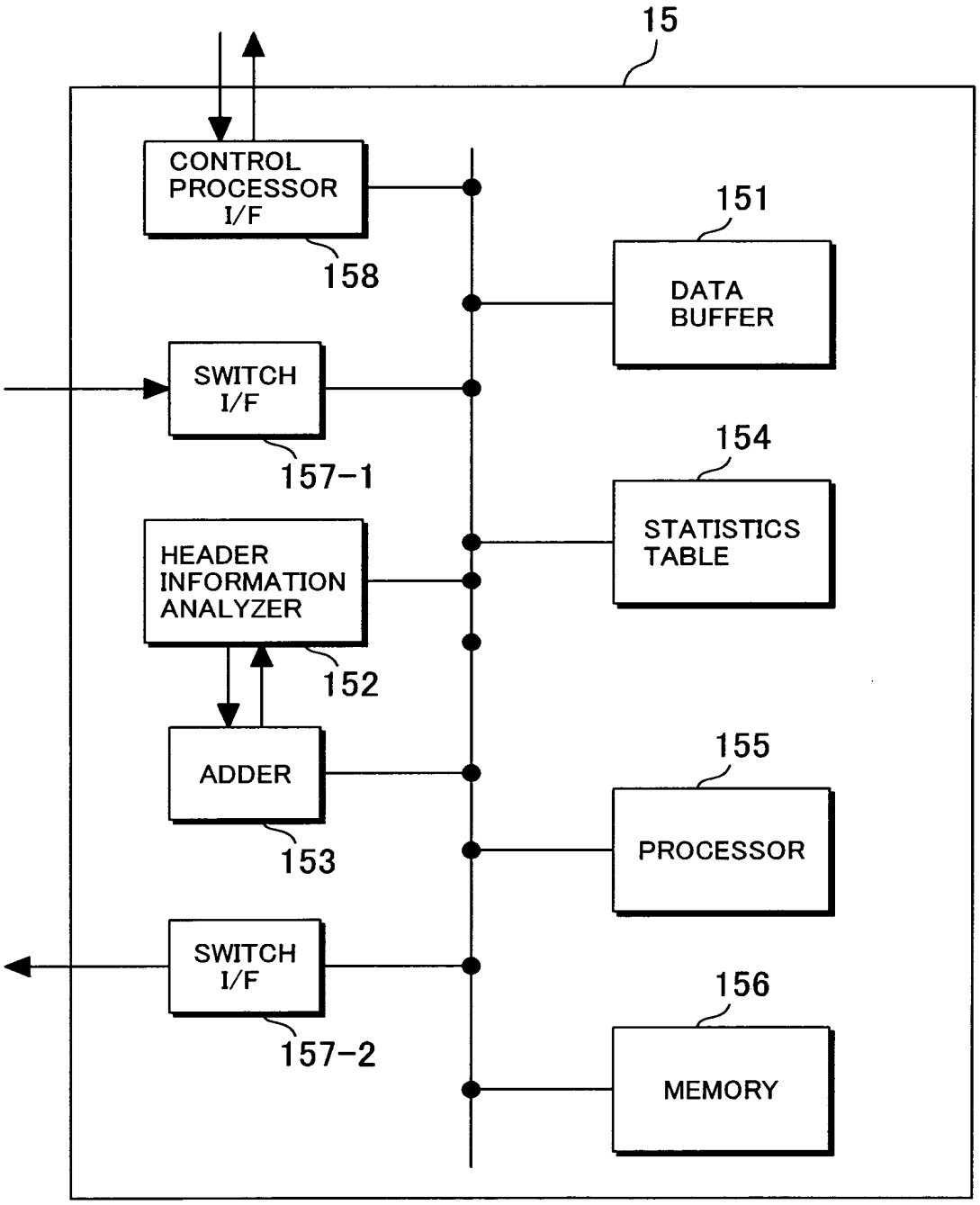

15
CONTROL PROCESSOR I/F
158
151
DATA BUFFER
SWITCH I/F
157-1
154
STATISTICS TABLE
HEADER INFORMATION ANALYZER
152
ADDER
153
155
PROCESSOR
SWITCH I/F
157-2
156
MEMORY

FIG.5

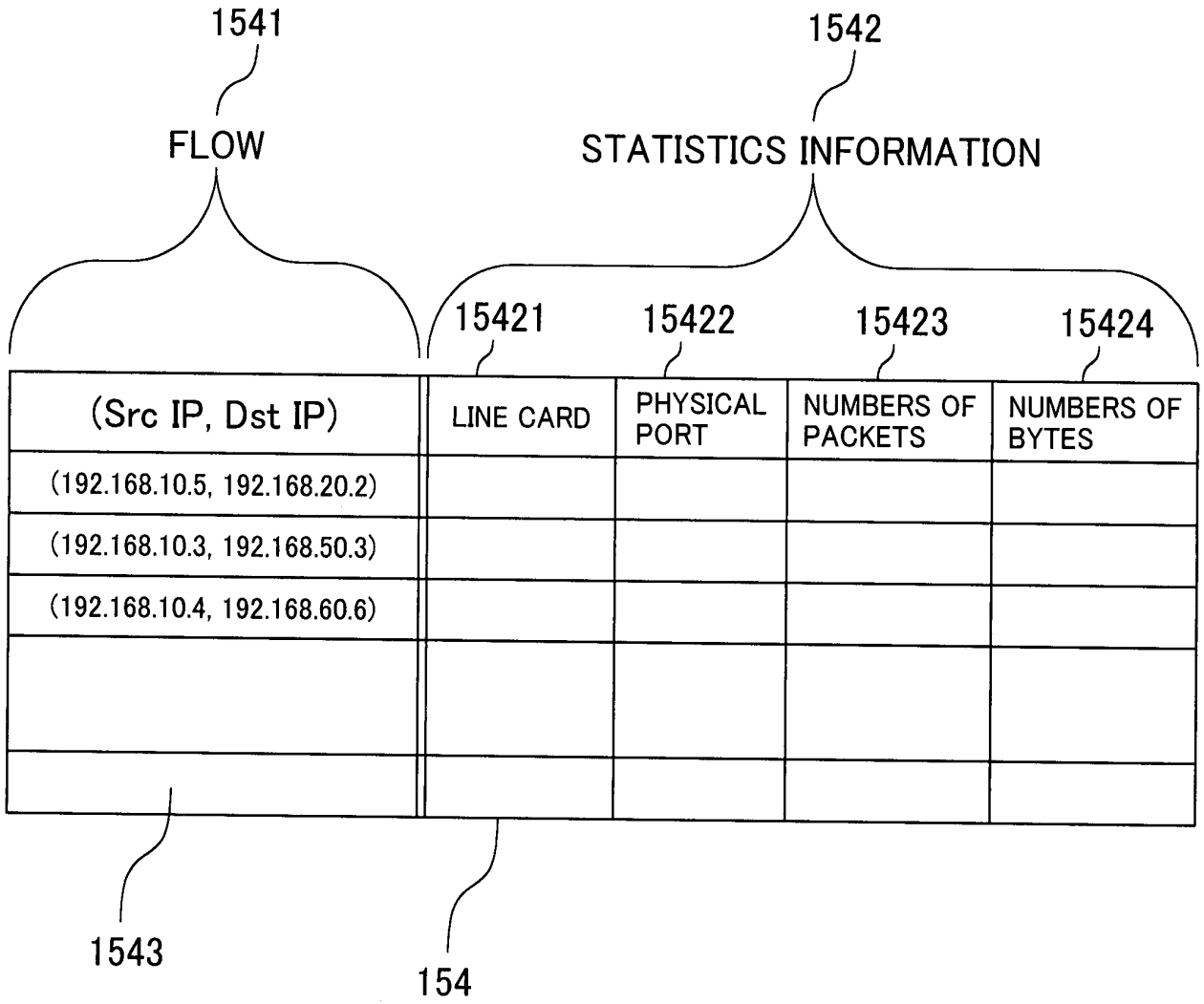

1541
1542
FLOW
STATISTICS INFORMATION
15421
15422
15423
15424
(Src IP, Dst IP)
LINE CARD
PHYSICAL PORT
NUMBERS OF PACKETS
NUMBERS OF BYTES
(192.168.10.5, 192.168.20.2)
(192.168.10.3, 192.168.50.3)
(192.168.10.4, 192.168.60.6)
1543
154

FIG.6

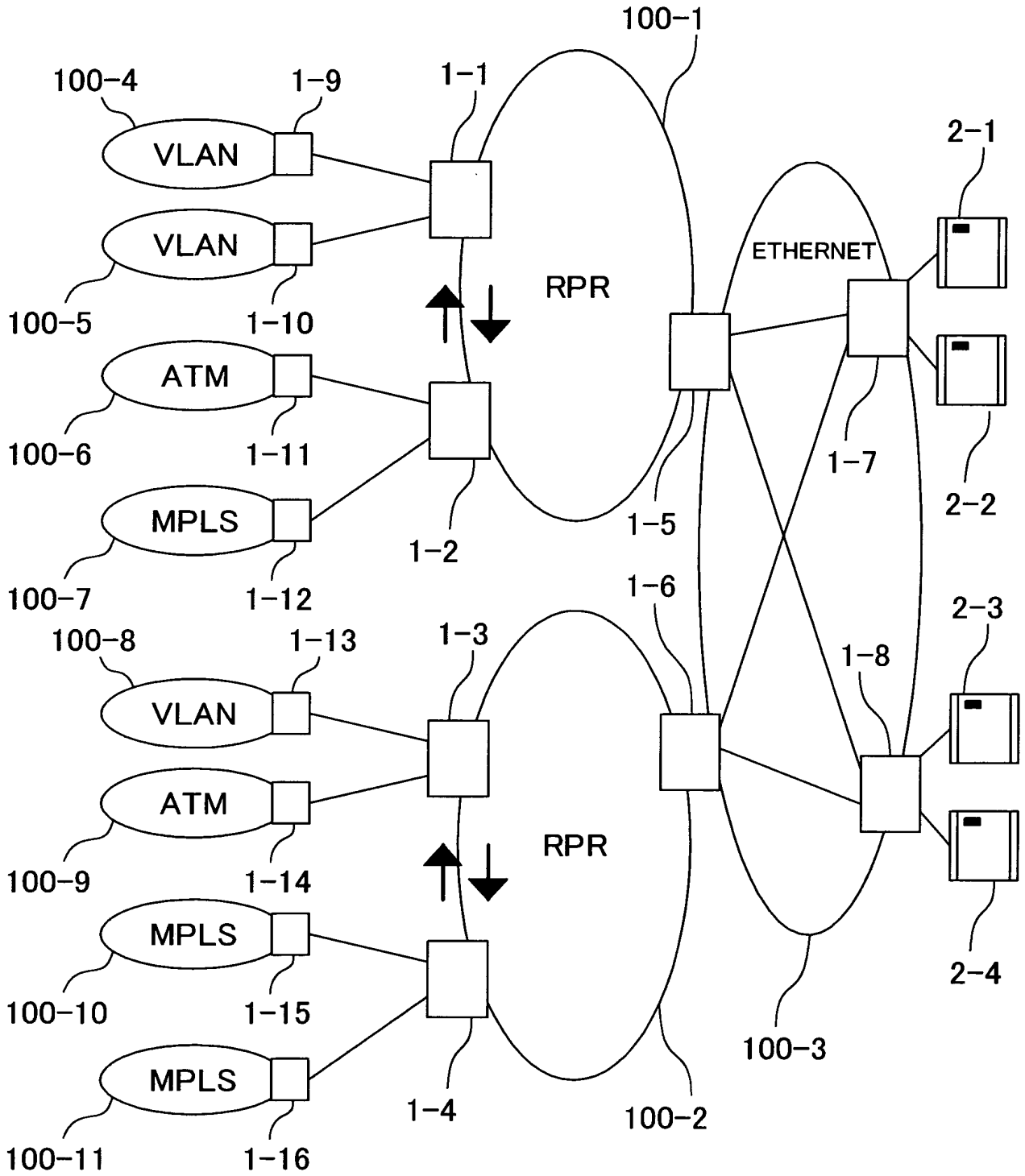

100-1
100-4
1-9
1-1
2-1
VLAN
VLAN
ETHERNET
RPR
100-5
1-10
ATM
100-6
1-11
1-7
2-2
MPLS
100-7
1-12
1-2
1-5
1-6
2-3
100-8
1-13
1-3
1-8
VLAN
ATM
RPR
100-9
1-14
MPLS
100-10
1-15
100-3
MPLS
1-4
100-2
100-11
1-16
2-4

FIG.7

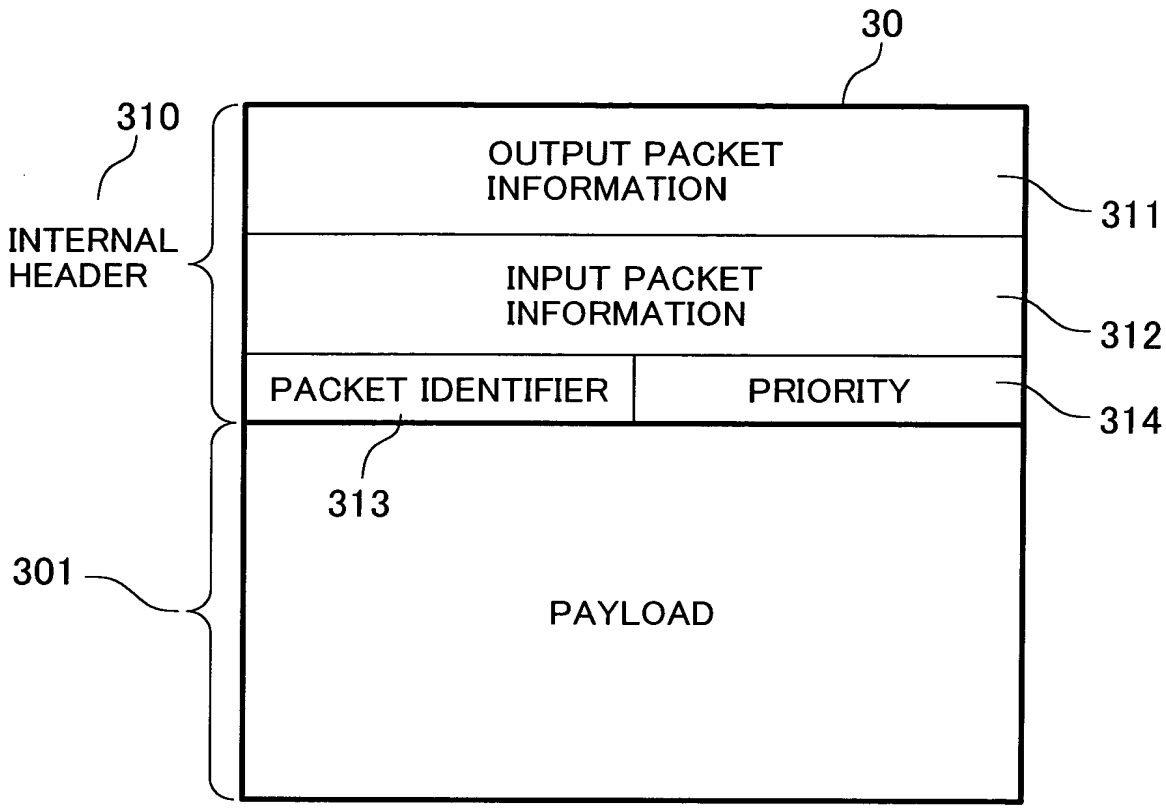

30
310
INTERNAL HEADER
OUTPUT PACKET INFORMATION
311
INPUT PACKET INFORMATION
312
PACKET IDENTIFIER
PRIORITY
314
313
301
PAYLOAD

FIG.8

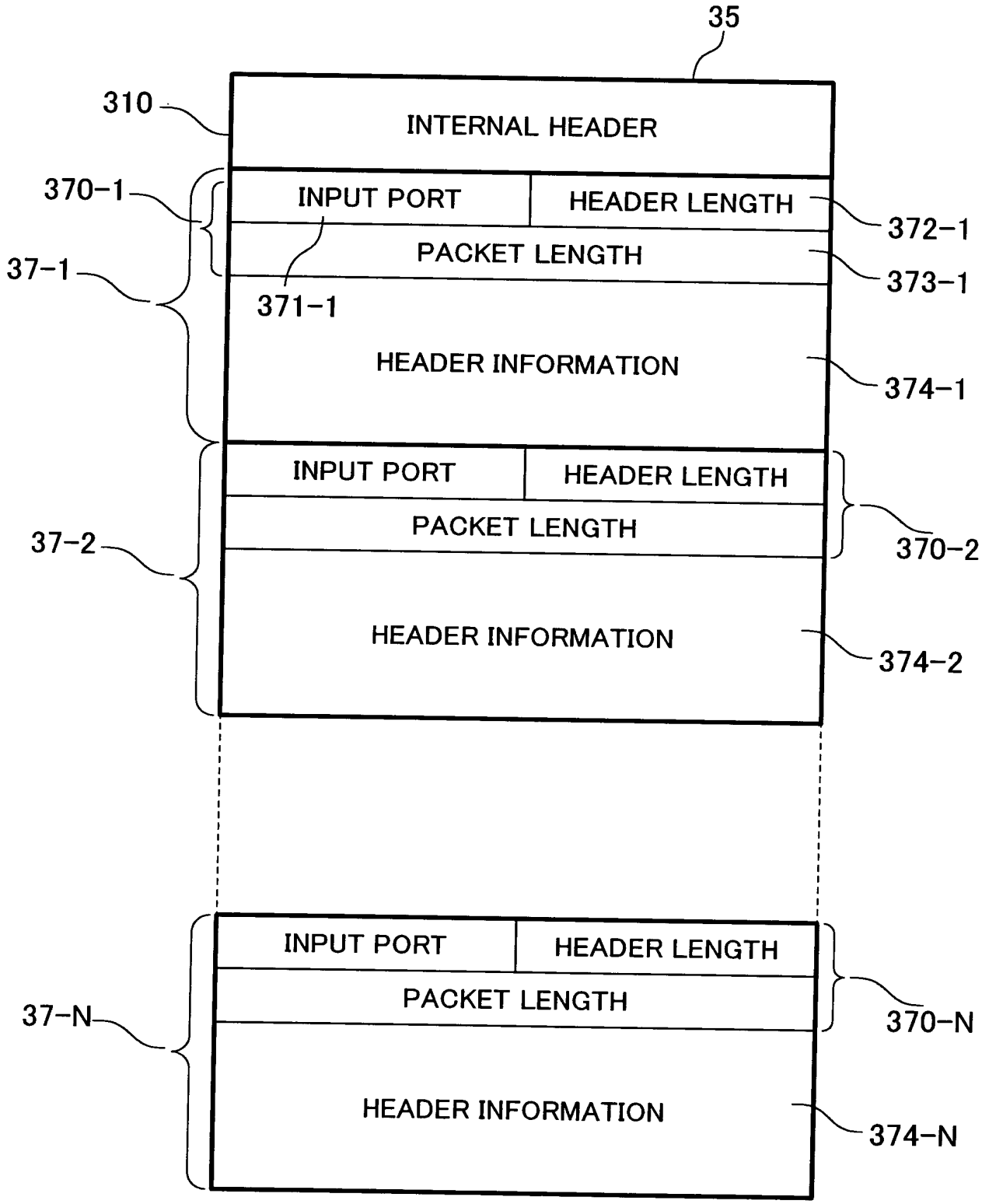

35
310
INTERNAL HEADER
370-1
INPUT PORT
HEADER LENGTH
372-1
PACKET LENGTH
373-1
37-1
371-1
HEADER INFORMATION
374-1
INPUT PORT
HEADER LENGTH
PACKET LENGTH
370-2
37-2
HEADER INFORMATION
374-2
INPUT PORT
HEADER LENGTH
PACKET LENGTH
370-N
37-N
HEADER INFORMATION
374-N

FIG.9

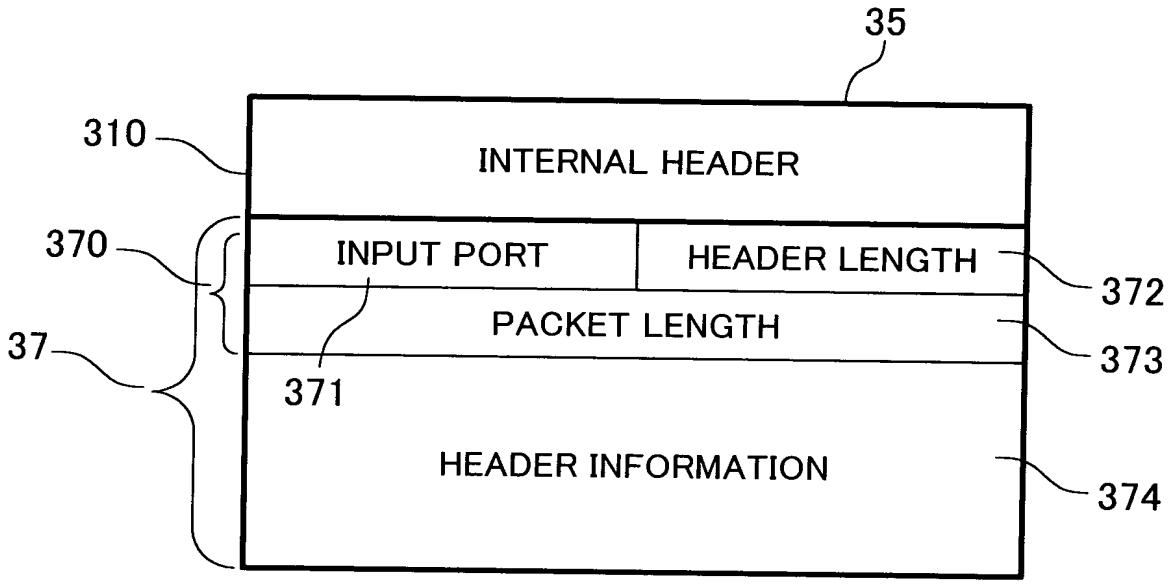

35
310
INTERNAL HEADER
370
INPUT PORT
HEADER LENGTH
372
PACKET LENGTH
373
37
371
HEADER INFORMATION
374

FIG.10

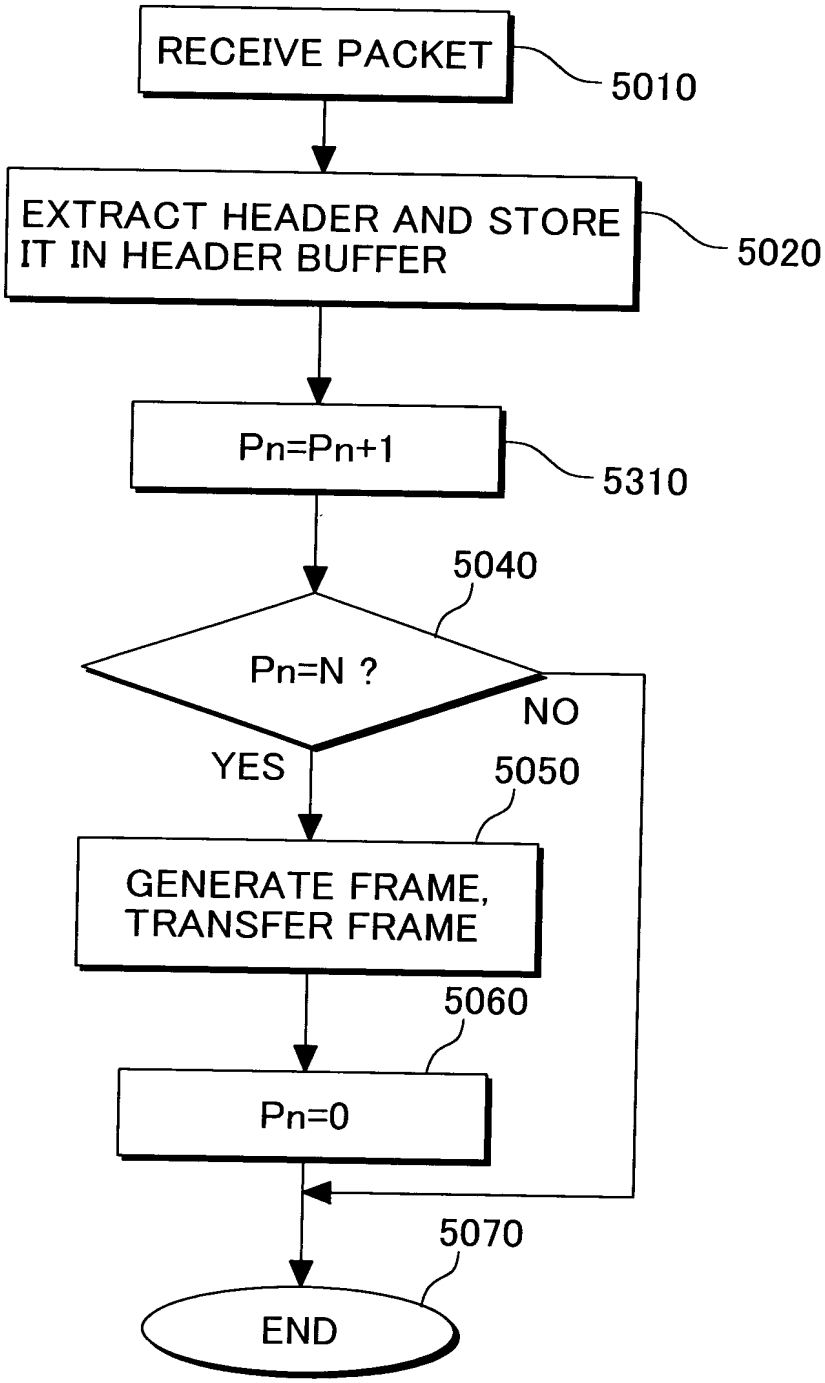

RECEIVE PACKET
5010
EXTRACT HEADER AND STORE IT IN HEADER BUFFER
5020
Pn=Pn+1
5310
5040
Pn=N ?
NO
YES
5050
GENERATE FRAME, TRANSFER FRAME
5060
Pn=0
5070
END

FIG.11

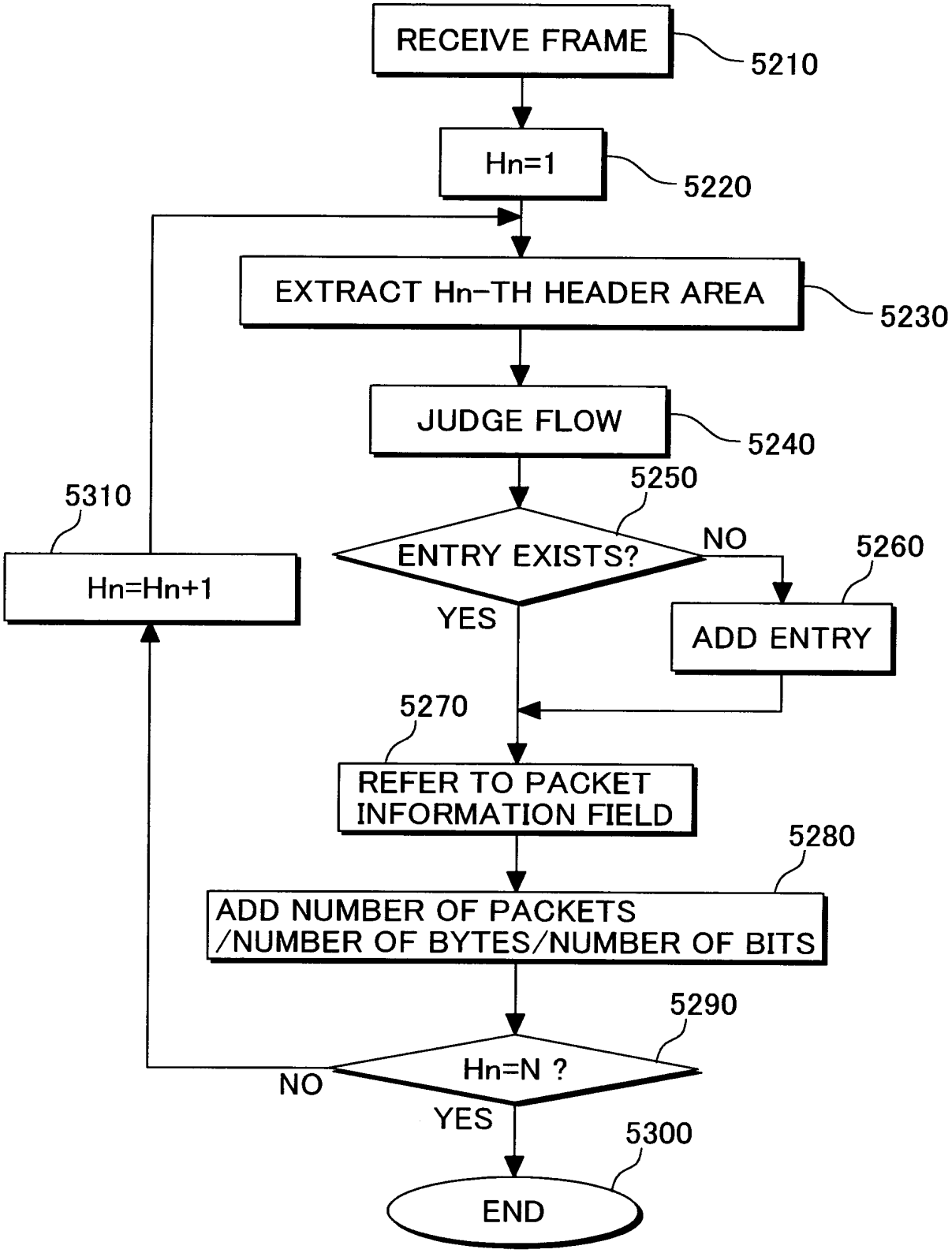

RECEIVE FRAME
5210
Hn=1
5220
EXTRACT Hn-TH HEADER AREA
5230
JUDGE FLOW
5240
5250
ENTRY EXISTS?
NO
5260
ADD ENTRY
YES
5310
Hn=Hn+1
5270
REFER TO PACKET INFORMATION FIELD
5280
ADD NUMBER OF PACKETS /NUMBER OF BYTES/NUMBER OF BITS
5290
Hn=N ?
NO
YES
5300
END

FIG.12

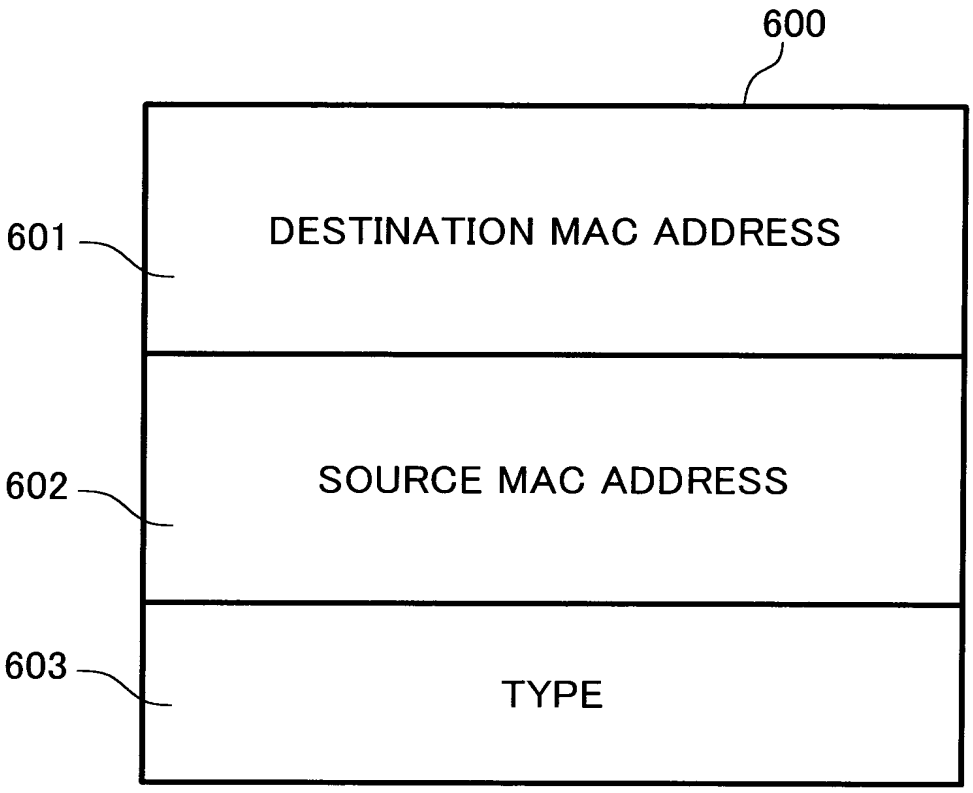

600
601
DESTINATION MAC ADDRESS
602
SOURCE MAC ADDRESS
603
TYPE

FIG.13

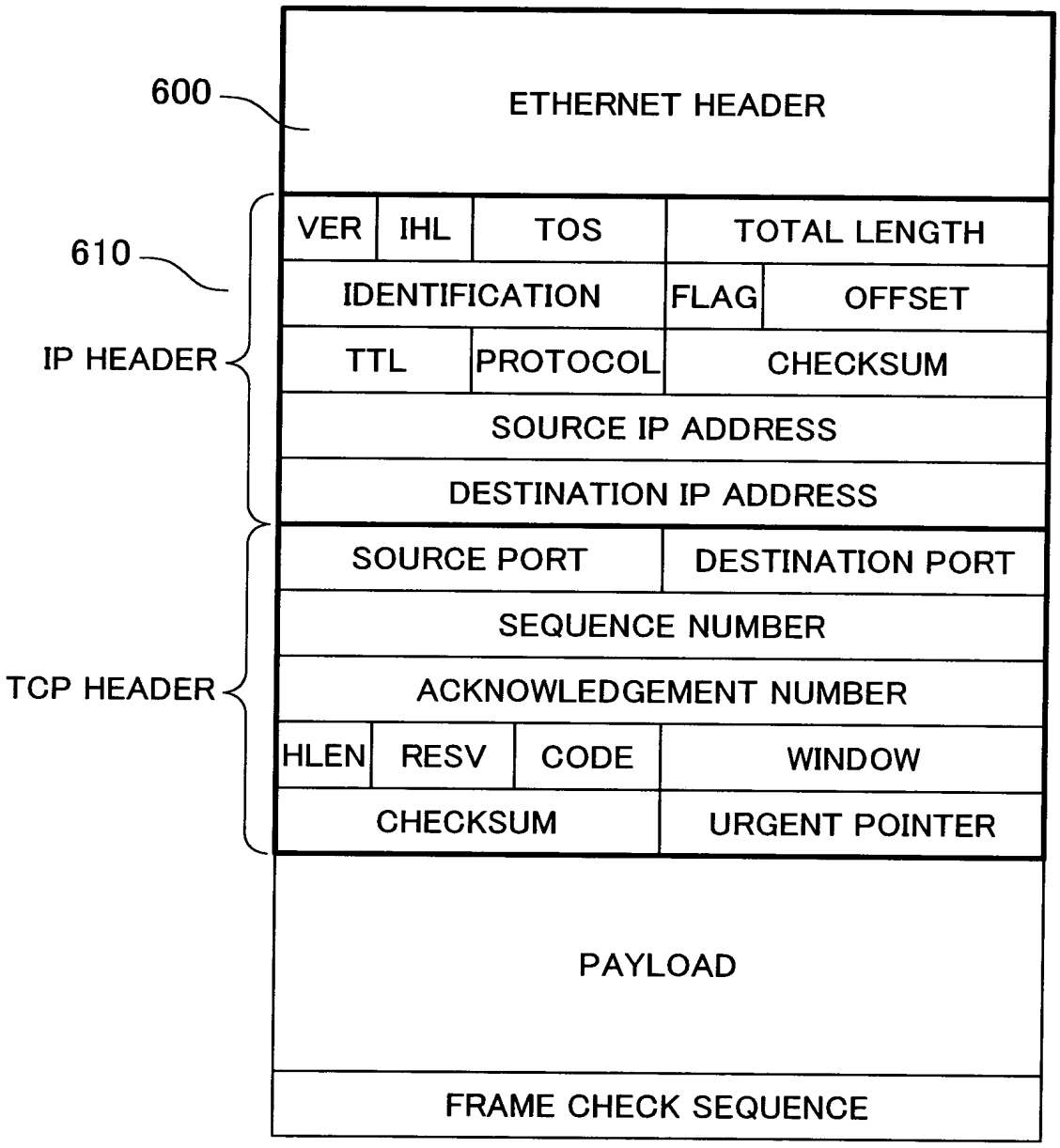

600
ETHERNET HEADER
610
IP HEADER
VER
IHL
TOS
TOTAL LENGTH
IDENTIFICATION
FLAG
OFFSET
TTL
PROTOCOL
CHECKSUM
SOURCE IP ADDRESS
DESTINATION IP ADDRESS
TCP HEADER
SOURCE PORT
DESTINATION PORT
SEQUENCE NUMBER
ACKNOWLEDGEMENT NUMBER
HLEN
RESV
CODE
WINDOW
CHECKSUM
URGENT POINTER
PAYLOAD
FRAME CHECK SEQUENCE

FIG.14

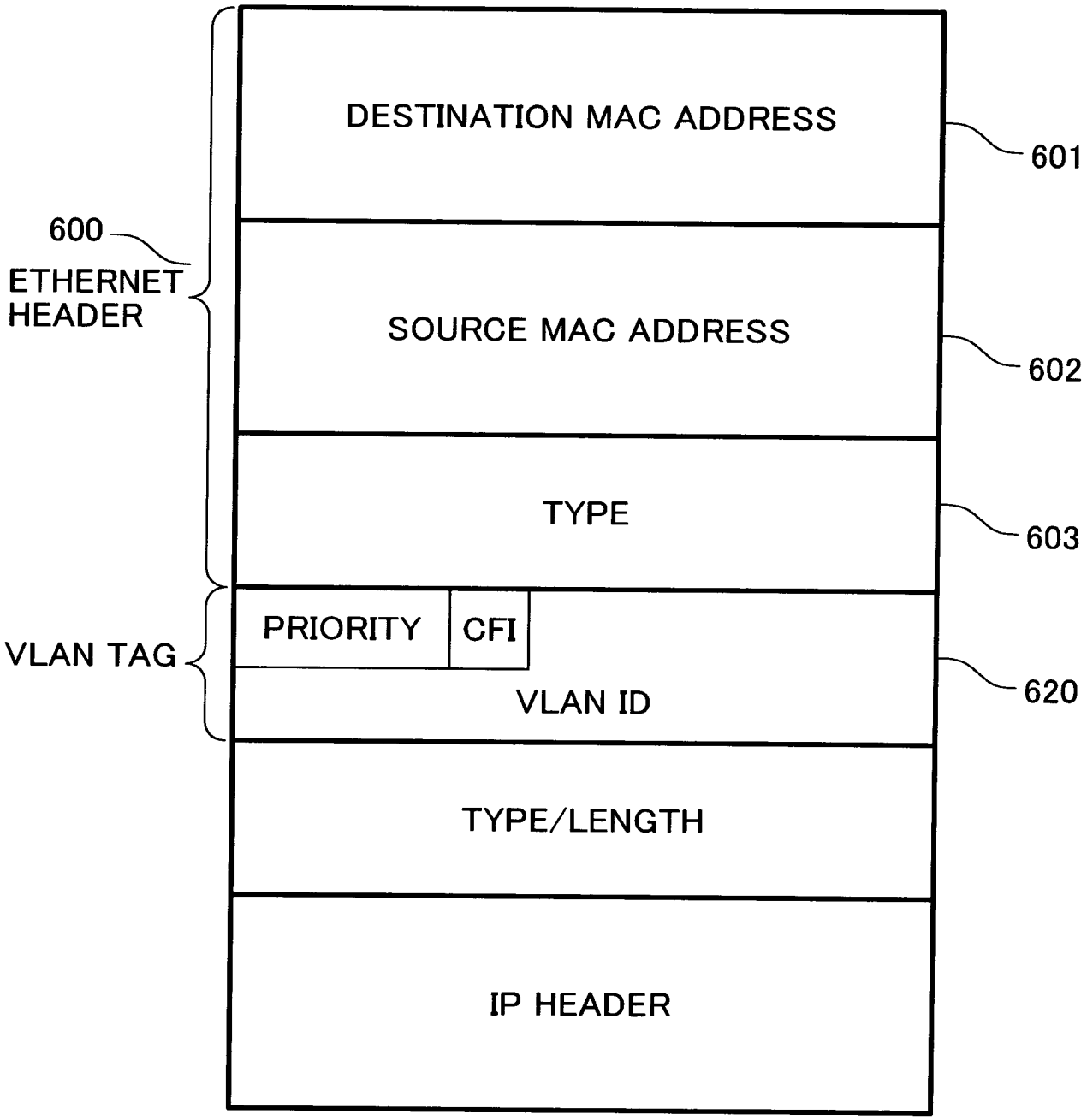

DESTINATION MAC ADDRESS
601
600
ETHERNET HEADER
SOURCE MAC ADDRESS
602
TYPE
603
VLAN TAG
PRIORITY
CFI
VLAN ID
620
TYPE/LENGTH
IP HEADER

FIG.15

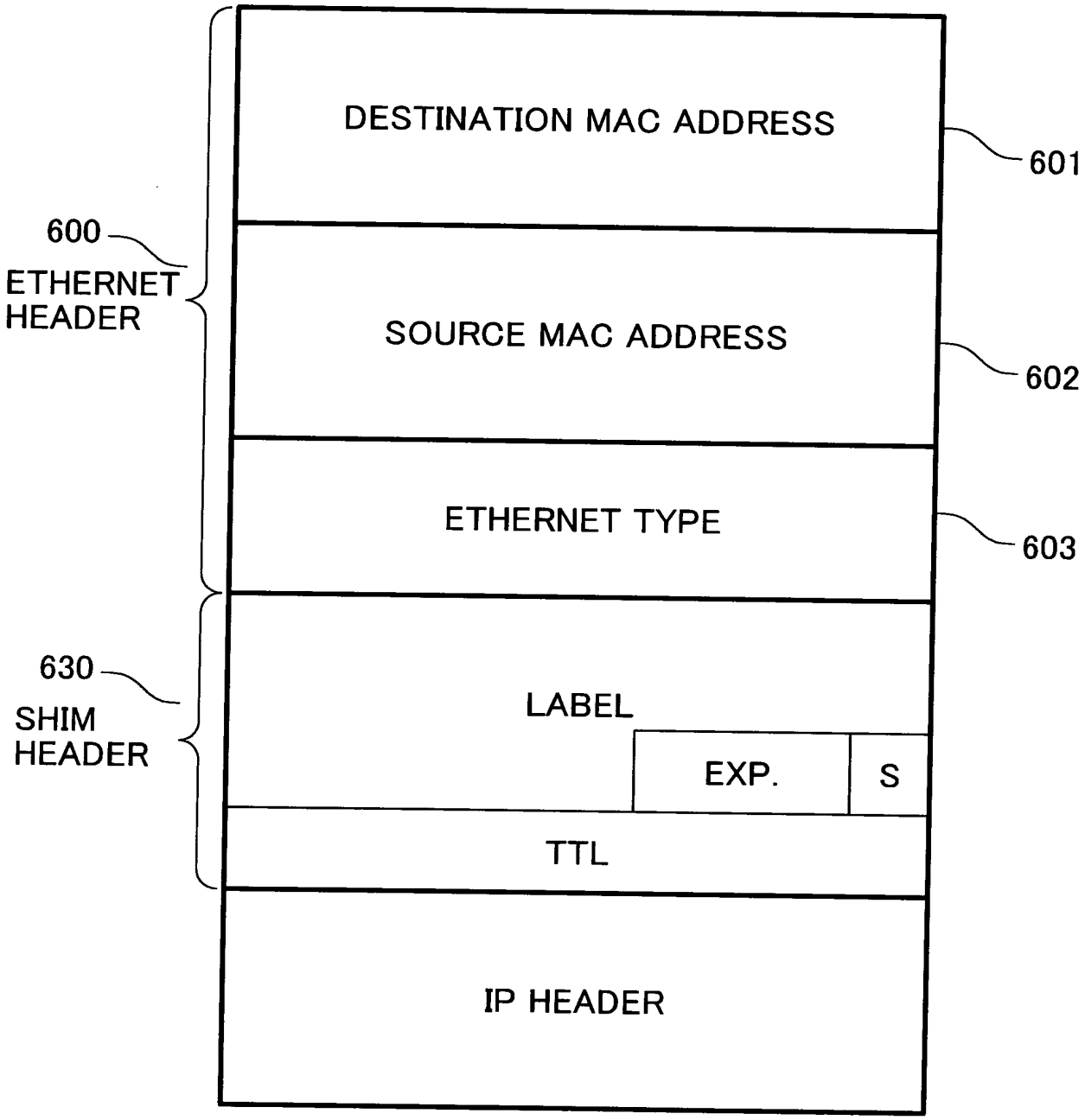

DESTINATION MAC ADDRESS
601
600
ETHERNET HEADER
SOURCE MAC ADDRESS
602
ETHERNET TYPE
603
630
SHIM HEADER
LABEL
EXP.
S
TTL
IP HEADER

FIG.16

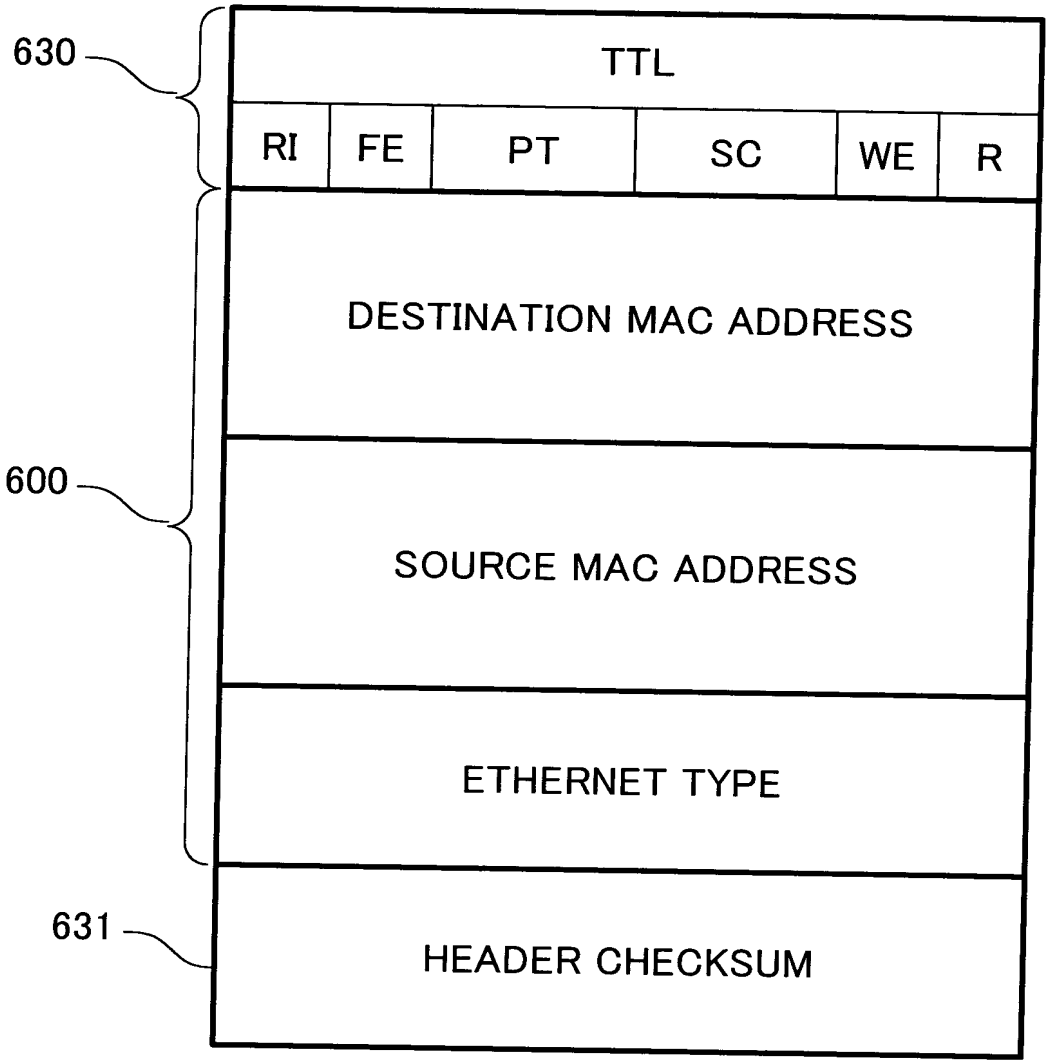

630
TTL
RI
FE
PT
SC
WE
R
DESTINATION MAC ADDRESS
600
SOURCE MAC ADDRESS
ETHERNET TYPE
631
HEADER CHECKSUM

FIG.17

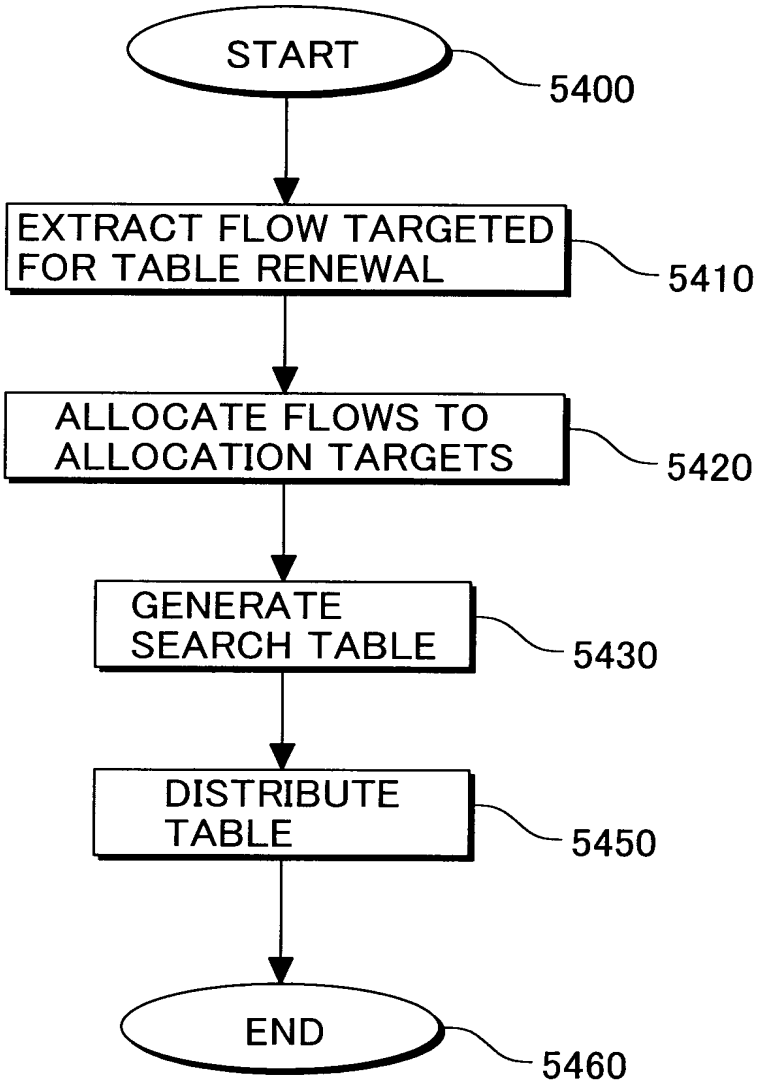

START
5400
EXTRACT FLOW TARGETED FOR TABLE RENEWAL
5410
ALLOCATE FLOWS TO ALLOCATION TARGETS
5420
GENERATE SEARCH TABLE
5430
DISTRIBUTE TABLE
5450
END
5460

FIG.18

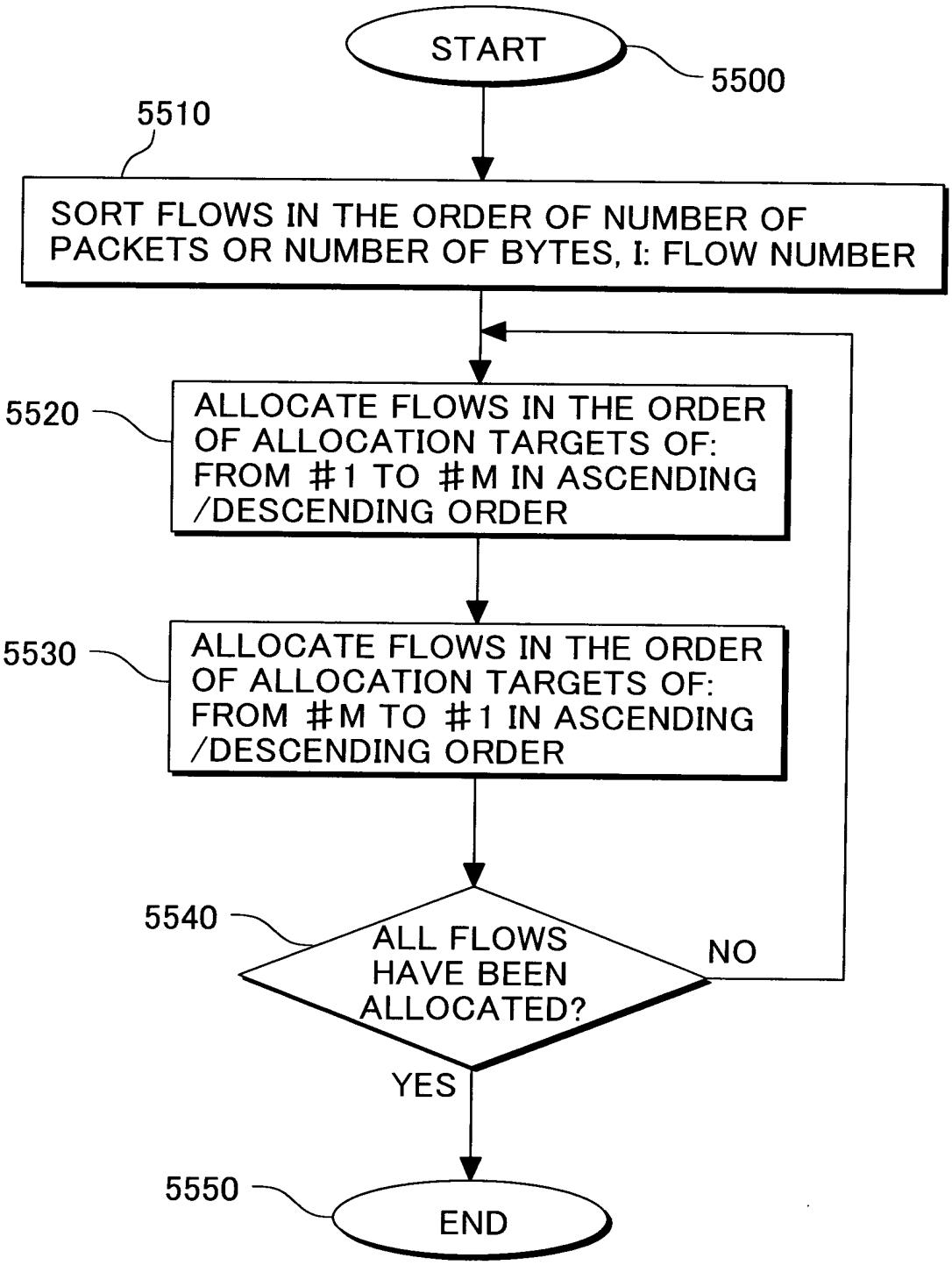

START
5500
5510
SORT FLOWS IN THE ORDER OF NUMBER OF PACKETS OR NUMBER OF BYTES, I: FLOW NUMBER
5520
ALLOCATE FLOWS IN THE ORDER OF ALLOCATION TARGETS OF: FROM #1 TO #M IN ASCENDING /DESCENDING ORDER
5530
ALLOCATE FLOWS IN THE ORDER OF ALLOCATION TARGETS OF: FROM #M TO #1 IN ASCENDING /DESCENDING ORDER
5540
ALL FLOWS HAVE BEEN ALLOCATED?
NO
YES
5550
END

FIG.19

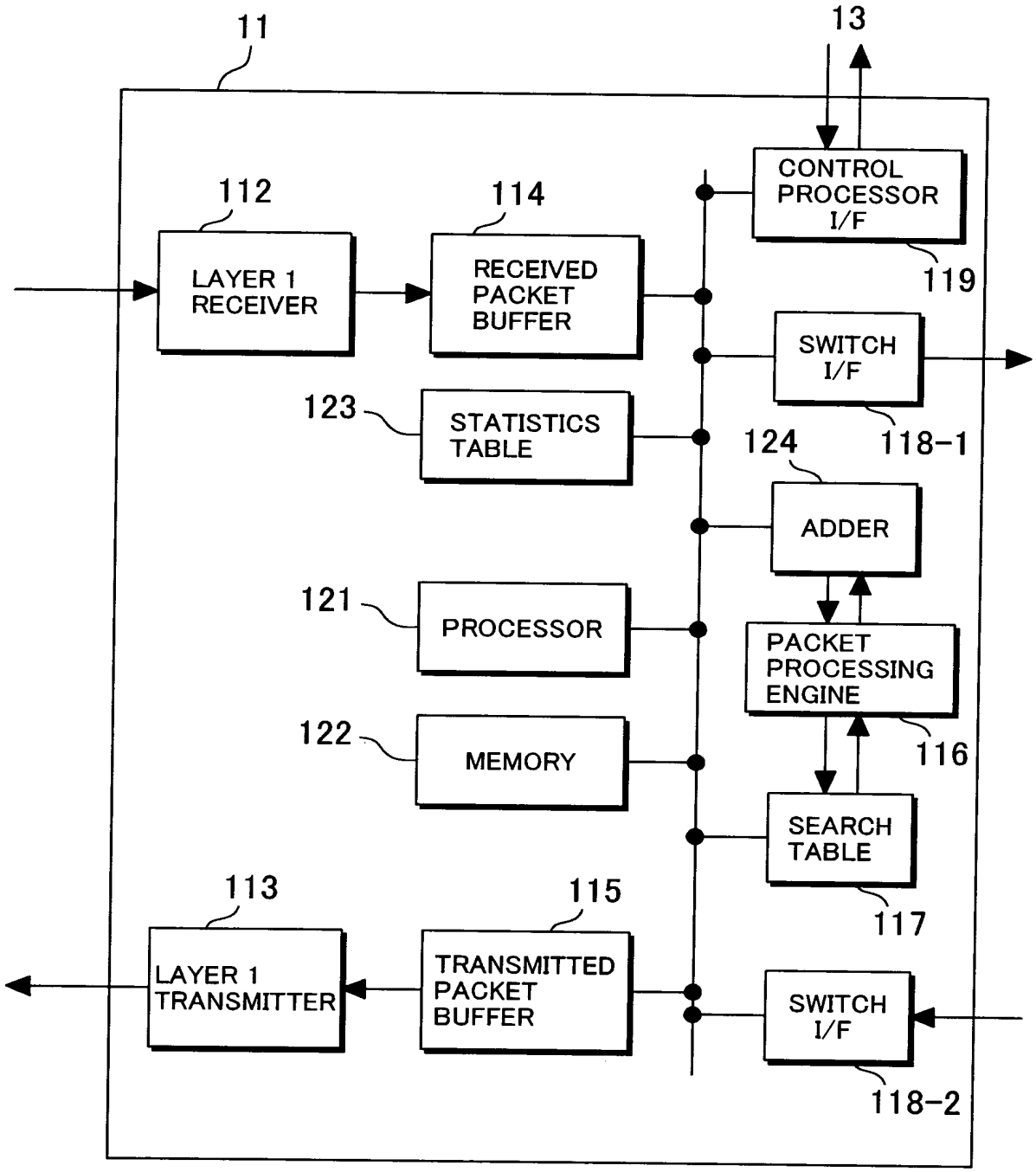

11
13
CONTROL PROCESSOR I/F
119
112
LAYER 1 RECEIVER
114
RECEIVED PACKET BUFFER
SWITCH I/F
118-1
123
STATISTICS TABLE
124
ADDER
121
PROCESSOR
PACKET PROCESSING ENGINE
116
122
MEMORY
SEARCH TABLE
117
113
LAYER 1 TRANSMITTER
115
TRANSMITTED PACKET BUFFER
SWITCH I/F
118-2

FIG.20

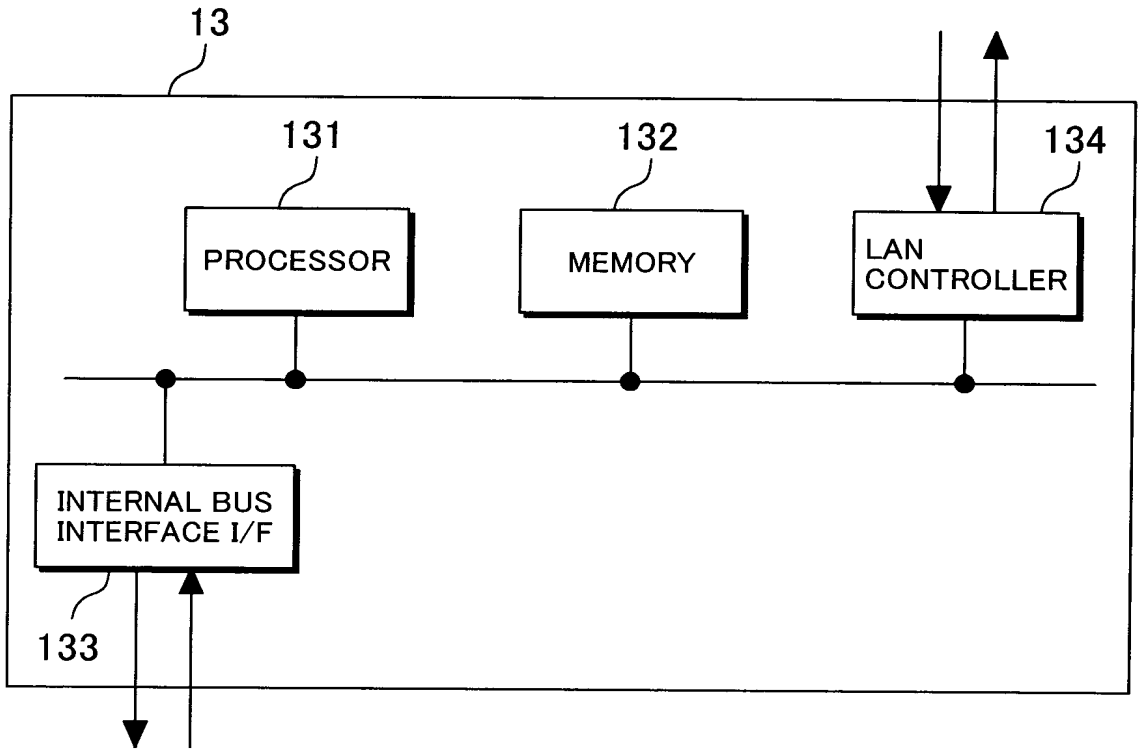

13
131
132
134
PROCESSOR
MEMORY
LAN
CONTROLLER
INTERNAL BUS
INTERFACE I/F
133

FIG.21

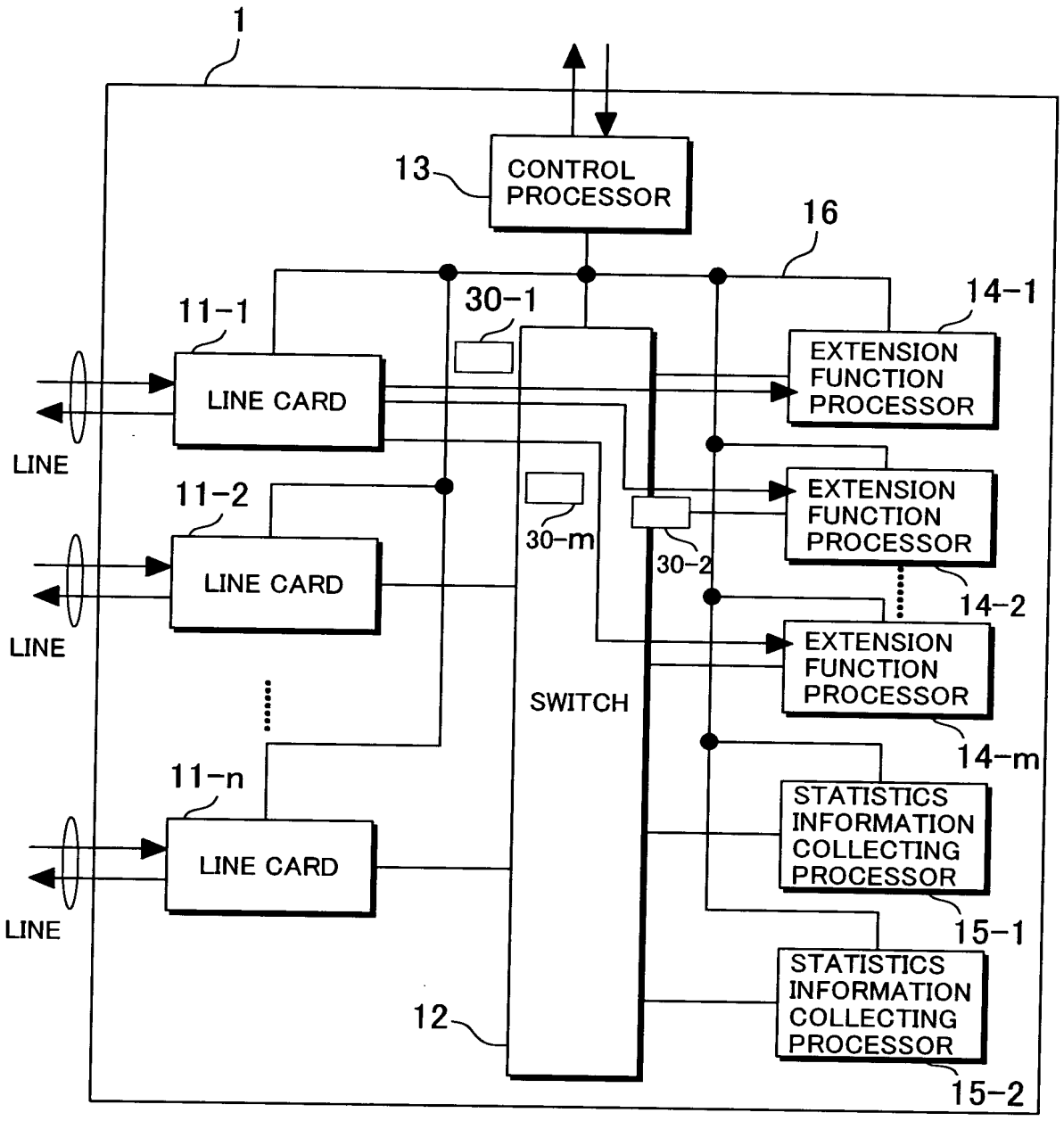

1
13
CONTROL PROCESSOR
16
11-1
30-1
14-1
LINE CARD
EXTENSION FUNCTION PROCESSOR
LINE
11-2
30-m
30-2
EXTENSION FUNCTION PROCESSOR
14-2
LINE CARD
LINE
SWITCH
EXTENSION FUNCTION PROCESSOR
14-m
11-n
STATISTICS INFORMATION COLLECTING PROCESSOR
15-1
LINE CARD
LINE
12
STATISTICS INFORMATION COLLECTING PROCESSOR
15-2

FIG.22

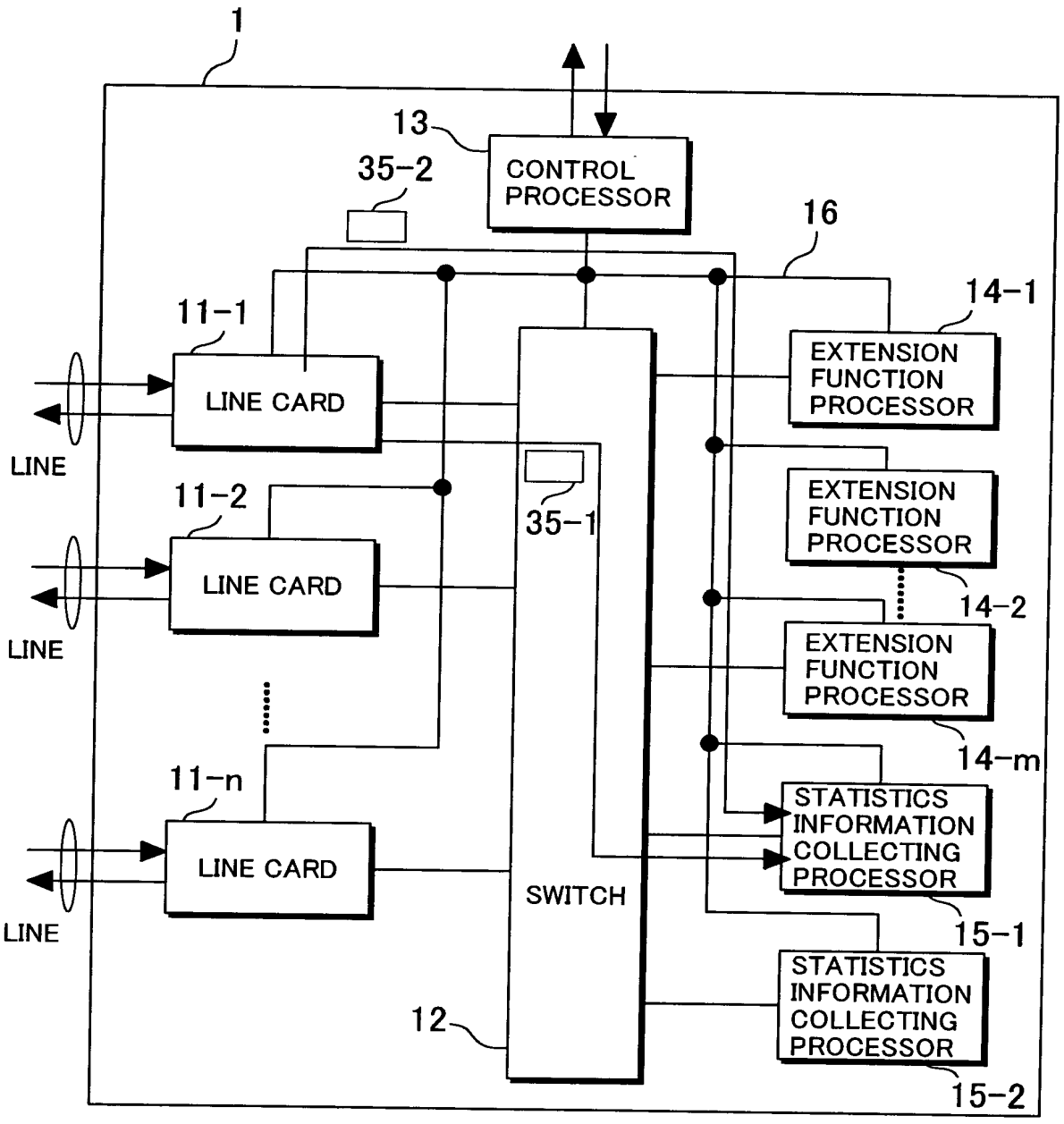

1
13
CONTROL PROCESSOR
35-2
16
14-1
EXTENSION FUNCTION PROCESSOR
11-1
LINE CARD
LINE
35-1
11-2
LINE CARD
LINE
EXTENSION FUNCTION PROCESSOR
14-2
EXTENSION FUNCTION PROCESSOR
14-m
11-n
LINE CARD
LINE
STATISTICS INFORMATION COLLECTING PROCESSOR
SWITCH
15-1
STATISTICS INFORMATION COLLECTING PROCESSOR
12
15-2

FIG.23

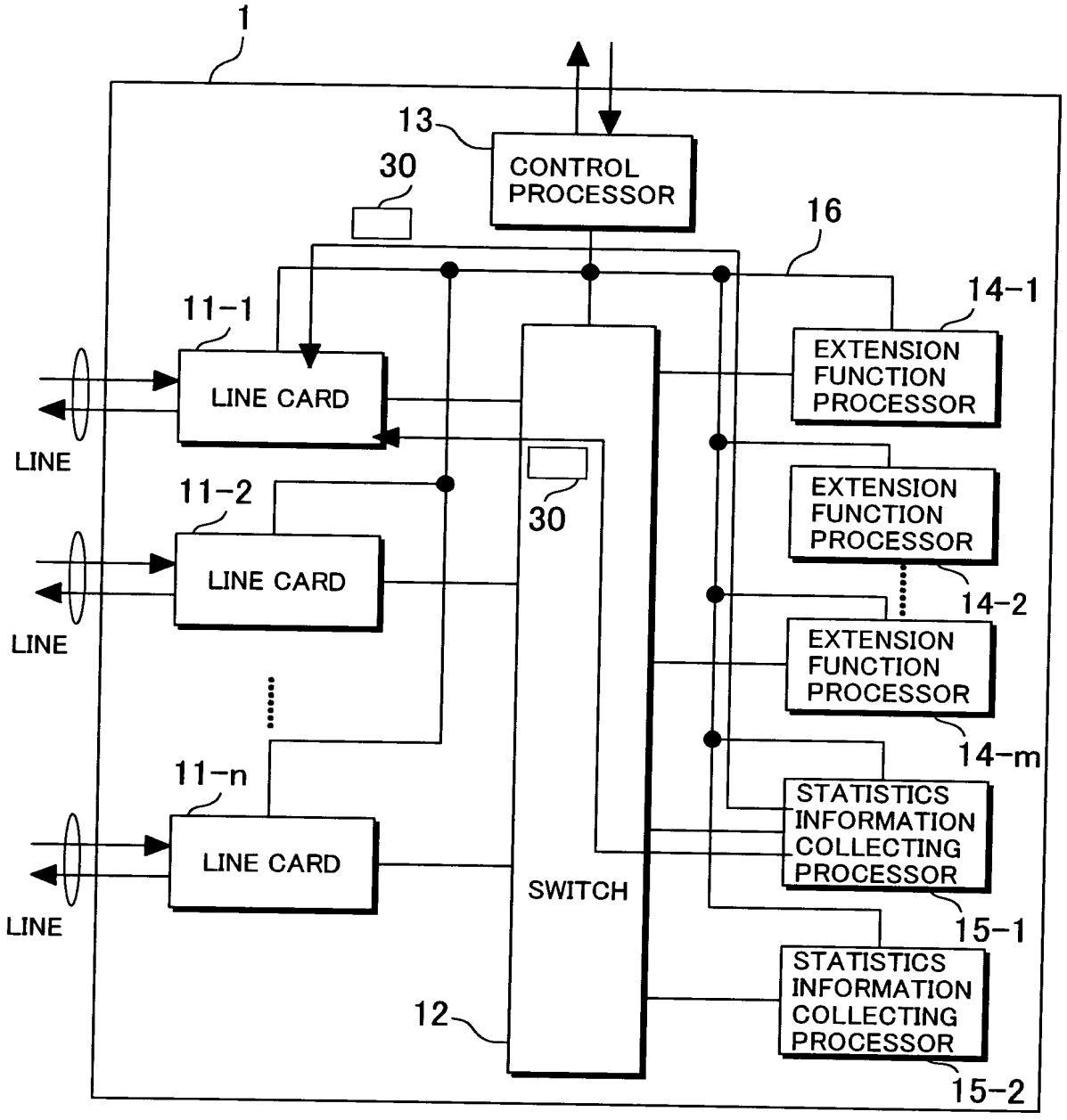

1
13
CONTROL PROCESSOR
30
16
14-1
EXTENSION FUNCTION PROCESSOR
11-1
LINE CARD
LINE
11-2
LINE CARD
LINE
30
EXTENSION FUNCTION PROCESSOR
14-2
EXTENSION FUNCTION PROCESSOR
14-m
11-n
LINE CARD
LINE
SWITCH
STATISTICS INFORMATION COLLECTING PROCESSOR
15-1
STATISTICS INFORMATION COLLECTING PROCESSOR
15-2
12

FIG.24

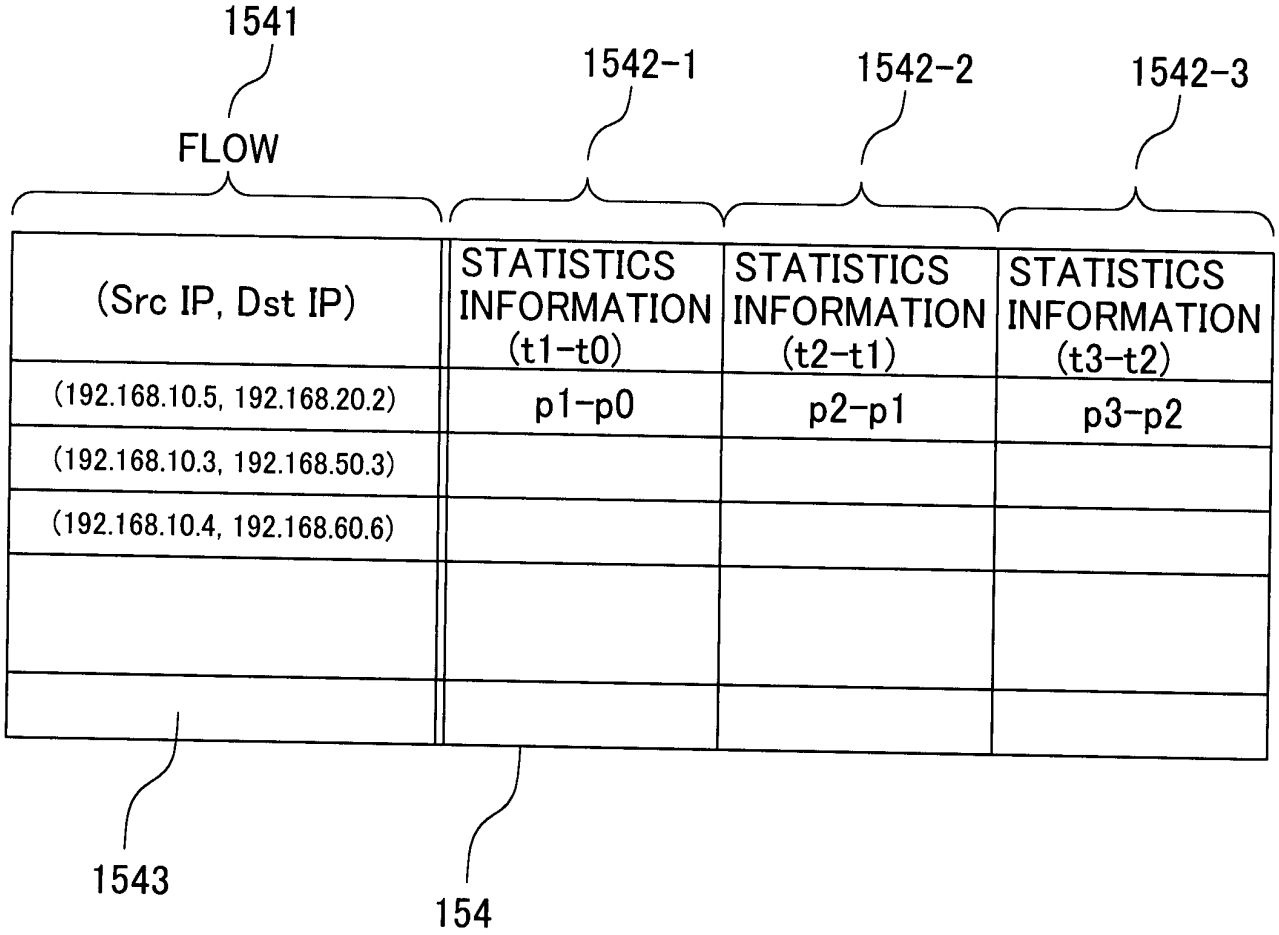
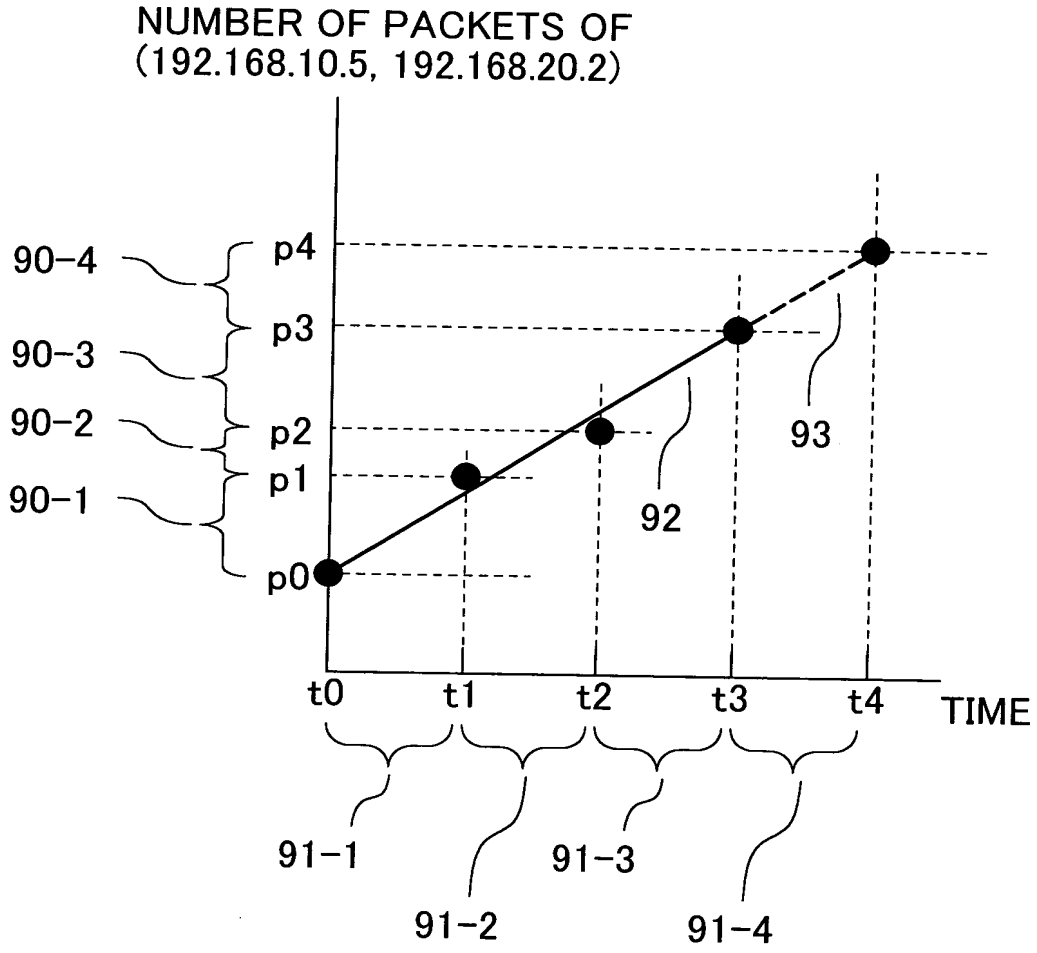

1541
1542-1
1542-2
1542-3
FLOW
(Src IP, Dst IP)
STATISTICS INFORMATION (t1-t0)
STATISTICS INFORMATION (t2-t1)
STATISTICS INFORMATION (t3-t2)
(192.168.10.5, 192.168.20.2)
p1-p0
p2-p1
p3-p2
(192.168.10.3, 192.168.50.3)
(192.168.10.4, 192.168.60.6)
1543
154

FIG.25


NUMBER OF PACKETS OF
(192.168.10.5, 192.168.20.2)
90-4
90-3
90-2
90-1
p4
p3
p2
p1
p0
92
93
t0
t1
t2
t3
t4
TIME
91-1
91-2
91-3
91-4